Surface plasmon polariton amplification in metal-semiconductor structures

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Microprocessor performance

Dhrystone 2.1
Release date: May 1988
Authors: R.P. Weicker and R. Richardson
Units: VAX MIPS (1 VAX MIPS is the speed of DEC VAX-11/780 computer)
Details: indicates general-purpose ("integer") performance
1 process
1 thread

Linear growth, not exponential!
Why?
Modern Electronics

Moore's law

Processor performance in

Dhrystone 2.1 (instructions per cycle)

Microprocessor performance in

Dhrystone 2.1 (VAX MIPS)

- Intel
- AMD

Core i7-2600K 3.4GHz (Turbo Boost 3.8GHz)
Core 2 Extreme X6800 2.93GHz
Core 2 Duo E8600 3.33GHz
Athlon 64 FX-57 2.8GHz
Athlon 1200MHz
AMD K6-2 400MHz
Phenom II X6 1100T 3.4GHz (Turbo Core 3.7GHz)

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Future of microprocessors with photonic technologies

Multicore Architecture
⊕ Very limited clock rate (several gigahertz)
⊕ Compact
⊕ Is not suited for many tasks such as recursion
⊕ Ready for the mass market, since it is based on the existing technologies
TODAY

All-Optical Data Processing
⊕ Extremely high clock rate (up to hundred TERAHERTZs)
⊕ Not compact
⊕ Is efficient for all tasks
⊕ Not ready for the mass market
IN FUTURE
Nvidia GeForce GTX 580

Number of CUDA Cores: 512
Performance: 1.58 TFLOPS

One executes $1.44 \times 10^{12}$ float point operations per second. After each 1-5 operations, one have to write or read information or transmit data to another core. So, the required bandwidth is 200-1000 GB/s.

Actual bandwidth equals 192.4 GB/s and memory interface width is 384-bit, i.e. 0.5 GB/s per line.
Twin-Wire Line Model

\[ C = \frac{\varepsilon_i l}{4 \ln(d/r)} \]
\[ L = 4l \ln(d/r) \]
\[ R_0 = \frac{l}{\pi r^2 \sigma} \]

Electrical interconnect limitations:
1) Propagation losses.
2) \( \tau = RC \) results is a delay and a rise time.
3) Miniaturizing the system doesn't reduce RC delay.

\[ B < B_0 \frac{d^2}{l^2} \], where \( B_0 < 10^{16} \text{ bit/s} \)

If \( d < \frac{l}{1000} \), than \( B < 1 \text{ GB/s} \)

Optical Interconnects

Utilizing on-chip optical interconnects, we will be able to achieve exaflop computing on a single chip.

Figure: http://domino.research.ibm.com/
Optical Interconnects

CMOS integrated silicon nanophotonics gives silicon nanophotonics devices a possibility to share the same silicon layer with silicon transistors and design On-Chip and Chip-to-Chip interconnects.

Transverse size of silicon waveguides is about 500nm x 500nm. So, they are quite compact, low loss and very fast. Bandwidth of silicon waveguides exceeds 10 Tb/s. Nevertheless, their size is limited by diffraction. However, we want a compact chip to use it in desktop computers and mobile devices.

Is is possible to propose a novel approach?

Requirements:
- More compact
- The same bandwidth
- The same delays
\[ \varepsilon_1(\omega) = \varepsilon_r - \frac{\omega_p^2}{\omega^2 + i \Gamma \omega} \]

\[ \varepsilon_1 = \text{Re}(\varepsilon_1) + i \text{Im}(\varepsilon_1) \]

\[ \text{Re}(\varepsilon_1) < 0 \]

\[ k_x = \text{Re}(k_x) + i \text{Im}(k_x) \] - SPP wavevector

\[ \kappa_i = \sqrt{k_x^2 - \left(\frac{\omega}{c}\right)^2} \varepsilon_i \] - penetration constants

\[ \rho_i = \frac{1}{\text{Re}(\kappa_i)} \] penetration depths

\[ L_{\text{spp}} = \frac{1}{2 \text{Im}(k_x)} \] propagation length

\[ \lambda_{\text{spp}} = \frac{2\pi}{\text{Re}(k_x)} \] SPP wavelength

\[ \kappa_1 \varepsilon_2 = - \kappa_2 \varepsilon_1 \] SPP dispersion
Plasmonics

SPP dispersion

$\kappa_1 \varepsilon_2 = -\kappa_2 \varepsilon_1$

SPP dispersion

1550 nm

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SPP dispersion

\[ \kappa_1 \varepsilon_2 = - \kappa_2 \varepsilon_1 \]

\[ \lambda = 1550 \text{ nm} \]

\[ \lambda_{\text{SPP}} \approx 1.5 \mu m \]

\[ L_{\text{SPP}} \approx 270 \mu m \]

\[ \rho_{\text{Air}} \approx 2.5 \mu m \]

\[ \rho_{\text{Au}} \approx 23 \text{ nm} \]
Dielectric Loaded SPP Waveguides (DLSPPWs)

Why DLSPPWs?

- Are easily fabricated
- Are easily coupled to other passive devices due to their planar structure
- High confinement and endurable propagation losses


$N_{\text{eff}}$ TM

$N_{\text{eff}}$ TM

$N_{\text{eff}}$ TM

$L_{\text{SPP}} < 10 \mu m$ at telecom wavelengths
High propagation losses due to Joule heating restrict the application of SPPs. Thus, one should increase the SPP propagation length, i.e. partially or fully compensate Joule losses. This can be done by using an active media placed near a metal surface. In recent years, a number of paper devoted to the SPP amplification have been published:


• and many other papers
Is it possible to design a COMPACT SPP waveguide with NEGLIGIBLY SMALL LOSSES?

Requirements:
- Compact pumping
- Full loss compensation
- Compatibility with compact SPP waveguides
- Single mode guiding

We answer YES!

Recently, we have proposed a novel scheme of SPP amplification that is based on a minority carrier injection in a metal–semiconductor diode. This scheme uses a compact electrical pumping instead of a bulky optical one. Moreover, the proposed technique can be used to obtain surface plasmon lasing and design spasers, actually nanoscale coherent light sources.

Usually, Schottky diodes are treated as majority carrier devices. However, the situation changes drastically when the metal work function $\Psi_M$ exceeds $\chi_e + \frac{E_g}{2}$, where $\chi_e$ and $E_g$ are the electron affinity and the band gap of the semiconductor, respectively. In this case, an inversion layer is formed. Under forward bias, holes are injected into the bulk of the semiconductor and recombine with electrons, that results in light emission. So, Schottky barriers can be used to design efficient and compact light- and plasmon-emitting diodes, but what about lasers and amplifiers? To design a laser, one should satisfy the condition for net stimulated emission or gain

$$F_e - F_h \geqslant \hbar \omega \geqslant E_g$$


$\psi_M = 5.4 \text{ eV}$
$\chi_e = 4.5 \text{ eV}$
$V_B = 0.9 \text{ eV} > E_g = 0.75 \text{ eV}$


We solve six nonlinear first order differential equations that describe the carrier behavior within the semiconductor:

\[
\begin{align*}
\frac{d\varphi}{dz} &= -E_z \\
\frac{dE_z}{dz} &= 4\pi e (p - n + N_d) / \varepsilon_{st} \\
\frac{dn}{dz} &= \frac{1}{eD_n} \left( J_n - \frac{\mu_n n}{D_n} E_z \right) \\
\frac{dp}{dz} &= -\frac{1}{eD_p} \left( J_p + \frac{\mu_p p}{D_p} E_z \right) \\
\frac{dJ_n}{dz} &= eU \\
\frac{dJ_p}{dz} &= -eU
\end{align*}
\]

where

\[
U = U_{\text{stim}} + U_{\text{spont}} + U_{\text{Auger}}
\]

together with six boundary conditions

\[
\begin{align*}
J_n \big|_{z=0} &= e \nu_{nr} (n \big|_{z=0} - n_0) \\
J_p \big|_{z=0} &= -e \nu_{pr} (p \big|_{z=0} - p_0) \\
\varphi \big|_{z=0} &= -\frac{\psi_M - \chi_e}{e} \\
\varphi \big|_{z=L} &= V + \frac{k_B T}{e} \ln \left( \frac{n_L}{N_c} \right) \\
n \big|_{z=L} &= n_L, \\
p \big|_{z=L} &= p_L
\end{align*}
\]

where

\[
\nu_{nr} \approx \frac{1}{4} \sqrt{\frac{8 k_B T}{\pi m_n}} ; \quad \nu_{pr} \approx \frac{1}{4} \sqrt{\frac{8 k_B T}{\pi m_p}}
\]

SPP Amplification

Stimulated emission and gain

\[ U_{\text{stim}}(z) = g \left( F_e(z), F_h(z) \right) S / \hbar \omega \]

\[ g = \frac{4 \pi^2 e^2}{c \bar{n} m_e^2 \omega} \left| M_b \right|^2 \int_{0}^{+\infty} \left| M_{\text{env}}(E, E - \hbar \omega) \right|^2 \rho_c(E - E_c) \rho_v(E_v - E + \hbar \omega) \times \left\{ \frac{1}{1 + \exp \left[ (E - F_e) / k_B T \right]} - \frac{1}{1 + \exp \left[ (E - \hbar \omega - F_h) / k_B T \right]} \right\} dE \]

- Gaussian Halperin-Lax band-tail (GHLBT) model
- Stern's envelope matrix element \( M_{\text{env}} \)

\[ L=400 \text{ nm}, \quad \psi_M=5.4 \text{ eV}, \]
\[ \varepsilon_{\text{st}}=13.94, \quad \varepsilon_{\text{opt}}=15.0, \]
\[ \chi_e=4.5 \text{ eV}, \quad E_g=0.75 \text{ eV} \]

that correspond to Ga\(_{0.47}\)In\(_{0.53}\)As at \( T=300 \text{ K} \), donor concentration \( N_d=4.3 \times 10^{18} \text{ cm}^{-3}, \quad \hbar \omega=0.73 \text{ eV} \) (\( \lambda=1.7 \mu\text{m} \)).
Stimulated emission and gain

$$U_{\text{stim}}(z) = g \left( F_e(z), F_h(z) \right) S / \hbar \omega$$

$$g = \frac{4 \pi^2 e^2}{c \bar{n} m_e^2 \omega} \left| M_b \right|^2 \int_0^+ \left| M_{\text{env}}(E, E - \hbar \omega) \right|^2 \rho_c(E - E_c) \rho_v(E_v - E + \hbar \omega) \times \left\{ \frac{1}{1 + \exp[(E - F_e)/k_B T]} - \frac{1}{1 + \exp[(E - \hbar \omega - F_h)/k_B T]} \right\} dE$$

$$\approx 8.76 \times 10^{-16} \left( \min(n, p) - 3.7 \times 10^{16} \right)$$

$L=400 \ \text{nm}, \ \psi_M=5.4 \ \text{eV},$

$\varepsilon_{\text{st}}=13.94, \ \varepsilon_{\text{opt}}=15.0,$

$\chi_e=4.5 \ \text{eV}, \ E_g=0.75 \ \text{eV}$ that correspond to Ga$_{0.47}$In$_{0.53}$As at $T=300 \ \text{K},$ donor concentration $N_d=4.3 \times 10^{18} \ \text{cm}^{-3}, \ \hbar \omega=0.73 \ \text{eV}$ ($\lambda=1.7 \ \mu\text{m}$).
Without gain: $2\text{Im}\beta = 1630 \text{ cm}^{-1}$

With gain: $2\text{Im}\beta = -150 \text{ cm}^{-1}$ (at $V=1.07 \text{ V}$), so we have an amplification regime
What about of shrinking the lateral (y) dimension?

There are no fundamental limitations for shrinking the lateral (y) dimension of the considered structure down to several hundred nanometers. Our structure has only two characteristic dimensions: thickness of the inversion layer and thickness of the depletion region. Both of them are appreciably less than 100 nm.

If the height $h$ of the semiconductor region is large enough, we can consider only plasmonic modes at the metal-semiconductor interface and obtain a situation similar to DLSPPWs.
What about of shrinking the lateral (y) dimension?

\[
\varepsilon_m = -141.6 + 15i \\
\varepsilon_d = 2.33 \\
\varepsilon_s = 13.69
\]
Summary

- Copper interconnects should be replaced by optical ones. However, despite the advantages of silicon photonics, even smaller interconnects are achievable with surface plasmon polariton based waveguides, which have the similar bandwidth and delays.
- SPP waveguides are quite lossy. However, one can partially or fully compensate losses using an active medium placed near the metal surface. Compact electrical pumping can allow to use SPP waveguides in nanoscale circuits and design core-to-core and on-core interconnects.
Thank you for your attention!

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